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(54) Embedded logic analyzer for a programmable logic device

(57) A technique for embedding a logic analyzer 260 in a programmable logic device 16 allows debugging of such a device in its actual operating conditions. A logic analyzer circuit is embedded within a PLD, it captures and stores logic signals, and it unloads these signals through an interface to be viewed on a computer. Using an electronic design automation (EDA) software tool running on a computer system, an engineer specifies signals of the PLD to be monitored, specifies the number of samples to be stored, and specifies a system clock signal and a trigger condition that will begin the acquisition of data. The EDA tool then automatically inserts the logic analyzer circuit into the electronic design of the PLD which is compiled and downloaded to configure the PLD. Using an interface connected between the PLD and the computer, the EDA tool communicates with the embedded logic analyzer in order to arm the circuit and to poll it until an acquisition has been made. The EDA tool then directs the logic analyzer to unload the data from its capture buffer and then displays the data on the computer. The logic analyzer circuit may then be rearmed to capture another sequence of sample values. The trigger condition may be changed without recompiling. The design may be recompiled with new logic analyzer parameters to debug a different portion.

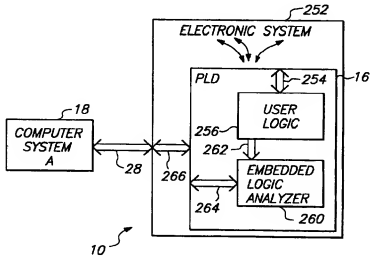

FIG. 5

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